IN THE CLAIMS

Please cancel claims 1 and 13-21 without prejudice or disclaimer.

Please amend claims 2-8 to read as follows:

2. A nonvolatile semiconductor memory device comprising:

a floating gate electrode formed on a semiconductor region via a first dielectric film;

a control gate electrode capacitively coupled with said floating gate electrode via a second dielectric film; and

a source region and a drain region that are formed in said semiconductor region on side regions of said floating gate electrode and control gate electrode;

wherein the end of said drain region faced with said source region has an embedded drain region extending toward said source region without reaching the surface of said semiconductor region, and

a channel region is formed near the surface of said semiconductor region directly above said embedded drain region such that the channel region reaches the surface of said semiconductor region.

3. The nonvolatile semiconductor memory device according to claim 2, further comprising an embedded region adjacent an upper area that is formed in an upper part of said embedded drain region in the semiconductor region and has a conduction type opposite to that of said drain region.

4. The nonvolatile semiconductor memory device according to claim 3, wherein an impurity concentration in said embedded region is higher than that in said semiconductor region.

5. The nonvolatile semiconductor memory device according to claim 3, wherein said embedded drain region has a conduction type opposite to that of said drain region and an impurity concentration lower than that in said embedded region.

Cont A3

6. The nonvolatile semiconductor memory device according to claim 2, wherein said embedded drain region has the same conduction type as that of said drain region.

7. The nonvolatile semiconductor memory device according to claim 2, further comprising an embedded region adjacent a lower area that is formed in the lower part of said embedded drain region in said semiconductor region and has a conduction type opposite to that of said drain region.

8. The nonvolatile semiconductor memory device according to claim 7, wherein an impurity concentration in said embedded region is higher than that in said semiconductor region.

SEE APPENDIX FOR CHANGES MADE TO SPECIFICATION AND CLAIMS

Please add the following new claims:

--22. A nonvolatile semiconductor memory device comprising:

a floating gate electrode formed on a semiconductor region via a first dielectric film;

a control gate electrode capacitively coupled with said floating gate electrode via a second dielectric film; and

a source region and a drain region that are formed in said semiconductor region on side regions of said floating gate electrode and control gate electrode;

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wherein the end of said drain region faced with said source region has an embedded drain region extending toward said source region without reaching the surface of said semiconductor region, and

a channel region is formed near the surface of said semiconductor region above said embedded drain region,

said nonvolatile semiconductor memory device further comprising an embedded region adjacent an upper area that is formed in an upper part of said embedded drain region in the semiconductor region and has a conduction type opposite to that of said drain region, wherein said embedded drain region has a conduction type opposite to that of said drain region and an impurity concentration lower than that in said embedded region.

23. A nonvolatile semiconductor memory device comprising:

a floating gate electrode formed on a semiconductor region via a first dielectric film;

a control gate electrode capacitively coupled with said floating gate electrode via a second dielectric film; and

a source region and a drain region that are formed in said semiconductor region on side regions of said floating gate electrode and control gate electrode;

wherein the end of said drain region faced with said source region has an embedded drain region extending toward said source region without reaching the surface of said semiconductor region, and

a channel region is formed near the surface of said semiconductor region above said embedded drain region,

said nonvolatile semiconductor memory device further comprising an embedded region adjacent a lower area that is formed in the lower part of said embedded drain region in said semiconductor region and has a conduction type opposite to that of said drain region.

24. The nonvolatile semiconductor memory device according to claim 23, wherein an impurity concentration in said embedded region is higher than that in said semiconductor region.

25. A nonvolatile semiconductor memory device comprising:

a floating gate electrode formed on a semiconductor region via a first dielectric film;

a control gate electrode capacitively coupled with said floating gate electrode via a second dielectric film; and

a source region and a drain region that are formed in said semiconductor region on side regions of said floating gate electrode and control gate electrode;

wherein the end of said drain region faced with said source region has an embedded drain region extending toward said source region without reaching the surface of said semiconductor region, and

a channel region is formed near the surface of said semiconductor region above said embedded drain region,

wherein said semiconductor region has a stepped portion, said floating gate electrode is formed astride said stepped portion, and

said drain region and embedded drain region are formed under a lower side of the said stepped portion.

Cont A4

26. A nonvolatile semiconductor memory device comprising:

a floating gate electrode formed on a semiconductor region via a first dielectric film;

a control gate electrode capacitively coupled with said floating gate electrode via a second dielectric film; and

a source region and a drain region that are formed in said semiconductor region on side regions of said floating gate electrode and control gate electrode;

wherein the end of said drain region faced with said source region has an embedded drain region extending toward said source region without reaching the surface of said semiconductor region, and

a channel region is formed near the surface of said semiconductor region above said embedded drain region,

wherein said control gate electrode is formed on said semiconductor region in the vicinity of the side of said floating gate electrode.

Cont A4

27. The nonvolatile semiconductor memory device according to claim 6, wherein said embedded drain region has an impurity concentration lower than that in said drain region.

28. The nonvolatile semiconductor memory device according to claim 2, wherein said drain region creates an electric field so that the carriers injected to said floating gate electrode are subject to an external force having an element directed from said semiconductor region to said floating gate electrode.--

REMARKS

The indication of allowable subject matter in claims 5, 7-9 and 12 is acknowledged and appreciated. Accordingly, claims 5, 7, 9 and 12 have been rewritten into independent form as new claims 22, 23 (new claim 24 corresponds to dependent claim 8), 25 and 26, respectively. It is therefore respectfully submitted that claims 22-26 are patentable over the cited prior art. Claim 2 is submitted to be patentable for the reasons that follow, and new claims 27 and 28 are submitted to be patentable based on their own merits by adding novel and non-obvious features to the combination.